LC-007

Proposal of Dependable Clock Signal Distribution

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1. Introduction

In deep submicron technologies, various noises generated by parasitic elements and signal changes come to influence circuit behaviors. Particularly, it is well known that a crosstalk noise induced by a parasitic capacitance between signal lines gives a large influence to a digital circuit [1]-[3]. This influence is called a crosstalk fault.

Measures against crosstalk faults in the digital circuit can be divided roughly into three methods; (1) Placement considering crosstalk faults [4]-[7], (2) Detection of crosstalk faults [8]-[11], (3) Security of normal behavior by dependable techniques [12]-[14]. In the first method, a circuit layout/routing design to prevent the generation of the crosstalk noise is carried out. However, it is difficult that its incidence is zero because of design constraints. In the second method, even if malfunction caused by the crosstalk fault is detected as a fault, it is difficult to feedback to a design phase because we may not find its cause. The third method is often realized by error detecting and correcting codes. This is effective for systematic data signals, for example data on a bus; however, it is difficult to apply it to general circuits.

A time redundancy method has been proposed as a dependable design for soft errors, which is enabled to catch proper data signals in the sequential circuit [15], [16]. However, crosstalk faults generated on the clock signal are not the object of the method. Metra et. al. have proposed on-line testing for detecting crosstalk faults generated on the clock signal [17], [18]. They assume the fault of a level sensitive clock signal (i.e., change in duty ratio of the clock signal). However, they do not consider the fault that generates an incorrect clock pulse.

The author considers that the introduction of a dependable (fault tolerant) technique is effective to measures against the crosstalk noise as follows. Since the crosstalk noise is generated by an intended parasitic element or other causes, we consider that it may be difficult to remove it perfectly. Besides, even if we regard the crosstalk noise itself or the influence of the noise as a fault, detecting it without missing is hard in general. Moreover, since the crosstalk noise is not necessarily generated, there is a possibility to cause the behavior of the intermittent fault. In particular, to detect the crosstalk noise, the synchronous sequential circuit must be tested considering the timing between clock and data signals. Therefore, detection of the crosstalk fault in the sequential circuit becomes harder. Thus, we consider that perfect elimination of the crosstalk noise is difficult. In this paper, we take the situation that the crosstalk noise is intermittently generated without intending. Therefore, we consider that circuit design with tolerance for the crosstalk noise is an effective method, which can secure the normal operation even if the crosstalk noise occurs.

In this paper, we target incorrect clock pulses induced by crosstalk faults because they cause malfunction of synchronous circuits composed of edge-triggered elements. Therefore, it is important to secure proper clock signal distribution. From the above-mentioned situation, we propose a method for generating clock signals and for detecting synchronous signals, which can secure the normal operation of synchronous circuits even if incorrect clock pulses are generated in the circuits. In addition, this method aims at having compatibility with conventional design. Particularly, if those circuits are added as adapter circuits to clocked elements (e.g., flip-flops) designed by the conventional method, we can easy build them in existing synchronous circuits.

This paper is organized as follows. Section 2 describes our idea for clock signal generation and its detection. In Section 3, we show an implementation example of the proposed method and simulation results. Section 4 concludes the paper.

2. Multiple clock pulse method

As described in the previous section, we assume the following conditions in this paper.

- Circuit type: Synchronous sequential circuits composed of edge-triggered/master-slave flip-flops (FFs)
- Clock signal: Clock pulse type
- Aggressor signal line: Signal lines except for clock signal line
- Victim signal line: Clock signal line

Two adjacent signal lines become candidates of an aggressor line and a victim line. In this case, if the value of a data signal line changes, an unintended crosstalk noise may be generated on the clock signal line because of a crosstalk fault (i.e., a crosstalk pulse occurs) (Figs.1(a) and 1(b)). If edge-triggered FFs recognize the crosstalk noise as a proper clock pulse, FFs correctly operate and finally the synchronous circuit causes a malfunction.

In order to operate correctly, data input to FFs must satisfy timing constraints called the set-up time and the hold time. Data signals need to be stable during periods of the set-up time and the hold time, and we therefore assume that the crosstalk noise (i.e., incorrect clock pulse) does not occur at those periods before and after the clock edge (Fig. 1(b)). In this section, although we assume the presence of only one incorrect crosstalk pulse, we describe two or more consecutive crosstalk pulses in the later section.

In order to eliminate/prevent the influence of the crosstalk fault, we must distinguish proper clock pulses and incorrect pulses caused by crosstalk faults. From the

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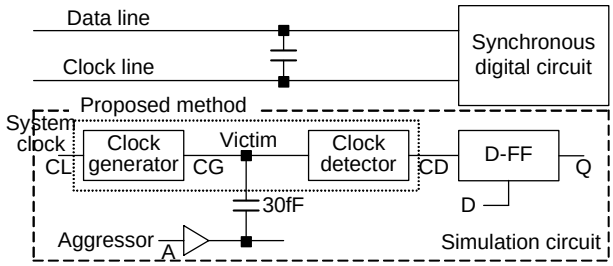

Fig. 1(a) Circuit example.

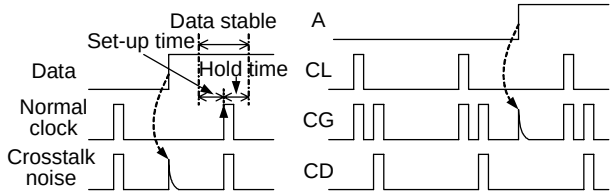

Fig. 1(b) Crosstalk noise. Fig. 1(c) Data and clock signals.

above discussion, it is difficult to distinguish them if we use a conventional single clock pulse system. In order to solve this problem, we therefore propose a multiple clock (double clock) pulse method to resist the crosstalk pulse. In this method, a clock generator produces double clock pulses regularly, and a clock detector recognizes them as proper clock signals. Figures 1(a) and 1(c) show this idea. The double pulse output (CG) from the clock generator shows the proper clock signal and it can be recognized as a clock signal (CD) by the clock detector. Thus, the clock detector produces one clock pulse for every one set of a double clock pulse. On the other hand, the single pulse shows the incorrect clock signal and it is blocked by the detector. We assume that both circuits are placed near the system clock generator and FFs as much as possible to prevent the generation of the crosstalk noise on the system clock and the FF input. For that purpose, the circuits are realized as adapter circuits; however, their implementation depends on a layout design. In the following section, we explain an implementation example of the proposed clock system.

3. Implementation and simulation results

3.1 Implementation

In order to realize the double clock pulse method, we design the circuit based on the following policies.

- The circuit structure is as simple as possible.
- The proposed method is applicable to existing design resources.

We design our method as adapter circuits to satisfy both policies because we can easy insert them into existing circuits if we realize them by adapter circuits.

The double clock generator is easy designed by using a delay circuit and a signal mixer circuit (OR gate) as shown in Fig. 2. The delay circuit consists of the inverter chain with capacitors. In this circuit, we consider that an input signal is a system clock. This means that if certain circuitries in a chip do not use the double clock pulse, they

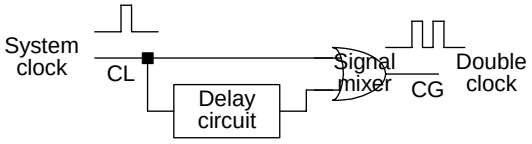

Fig. 2 Clock generator.

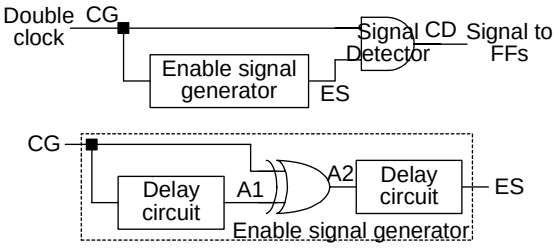

Fig. 3(a) Clock detector.

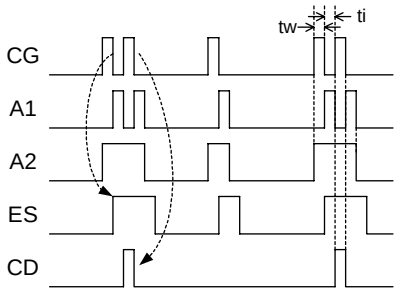

Fig. 3(b) Timing chart.

use the conventional single clock pulse that is supplied by the system clock.

On the other hand, there is a possibility that the clock detector for the double clock pulse is implemented by several designs. When we consider a double clock pulse to be two consecutive pulses, we must design new FFs that are triggered by two consecutive pulses. This does not satisfy our design policies. In order to apply the double clock signal to conventional FFs, we therefore consider the following function. The first pulse of the double clock pulse generates an enable signal (ES) to catch the next pulse and the second pulse is detected as an actual clock signal entering the FF. Figure 3 shows this function briefly. As shown there, when one double pulse (CG) enters the clock detector, one clock pulse (CD) is detected and it goes to FFs. If a single pulse that means the crosstalk noise enters the detector, the enable signal is generated; however, the clock pulse does not reach to FFs because the input signal of the detector already returns to zero.

The enable signal with the high level must return to zero before the next double clock signal is generated. In order to realize this function simply, we use a transition-triggered one shot as the enable signal generator because this circuit does not require a feedback signal [1]. The lower diagram of Fig. 3(a) shows this design example. Here, we assume the same width of the clock pulse and its interval, tw=ti, because of simple implementation (Fig. 3(b)). The delay circuit consists of the inverter chain with capacitors.

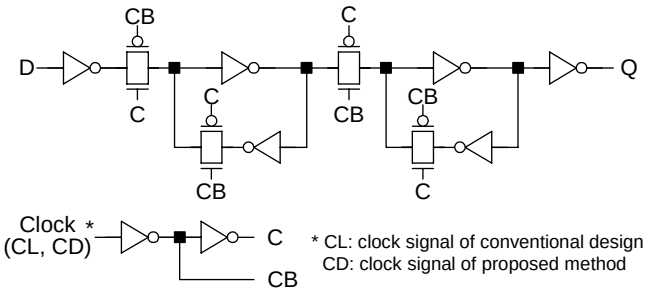

Fig. 4 Master-slave D-FF.

3.2 Simulation results

We verify the circuit function by circuit simulation. We use the following conditions in this simulation.

- TSMC 0.18um parameters of 1.8V-VDD [19]
- 100MHz and 300MHz clock frequencies
- Master-slave D-FF (Fig. 4)

The dashed line part of Fig. 1(a) shows the summary of a simulation circuit. To generate the crosstalk noise with enough amplitude, the aggressor signal must have an appropriate driving strength. Besides, to prevent signal degradation of the victim line when the signal of the aggressor line is stable, the crosstalk capacitor must be an appropriate value. To achieve those, we use the 3.3V-VDD driver for the aggressor line and the crosstalk capacitor of 30fF. We set the clock width tw to 0.3ns. Note that since the ring oscillator frequency of 31-stage for 1.8V-VDD is 328.75MHz [19], we expect that circuits designed by TSMC-0.18um operate at that frequency.

Figures 5 and 6 show simulation results at 300MHz, where symbols of signal lines are the same as Figs. 1 and 3. Figures 5(a) and 5(b) shows results of the conventional design with fault-free and faulty signals, respectively. Note that the victim line (clock line) is directly connected to the FF in the conventional design (see Fig. 1(a)). In Figure 5(b), crosstalk pulses are generated at 4.5ns, 7.8ns, and 11.1ns and the FF responds to them. As a result, the FF causes the incorrect operation. Figures 6(a) and 6(b) show results of the proposed method with fault-free and faulty signals, respectively. We find that even if the crosstalk noise is generated, the FF operates properly when the clock signal is supplied to the FF by the proposed method. Therefore, we can say that the double clock pulse method is effective for the crosstalk-induced pulse. The proposed circuit operates correctly in the range of 100MHz to 300MHz without design change.

3.3 Comments and future works

(1) So far, we assume the single crosstalk pulse and then we use the double clock pulse. However, multiple pulses of two or more may occur because of data change with different timing. For this case, we can use the similar method. As shown in Figs. 7 and 8, when the parallel or serial connection of signal generators and detectors is used, we can realize a triple or more clock pulse method that can be applied to the double or more crosstalk pulse.

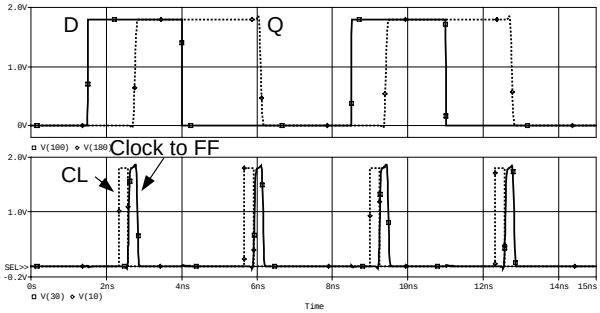

Fig. 5(a) Conventional method without crosstalk.

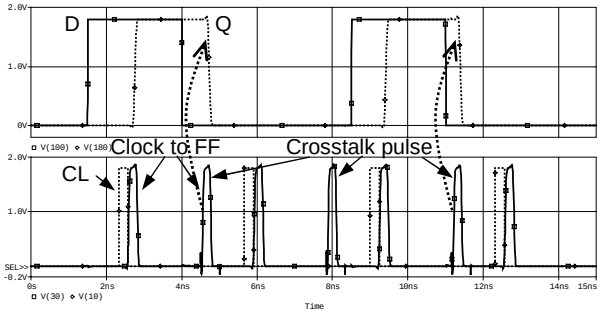

Fig. 5(b) Conventional method with crosstalk.

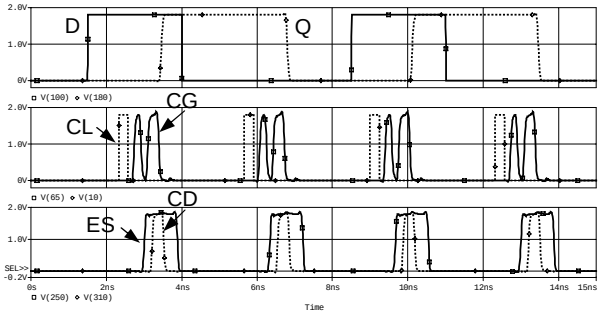

Fig. 6(a) Proposed method without crosstalk.

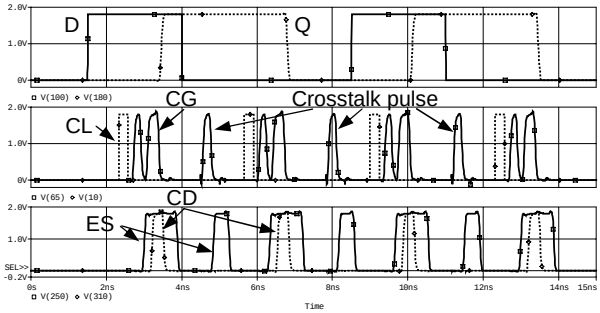

Fig. 6(b) Proposed method with crosstalk.

(2) The proposed method is realized as the adapter circuit as shown in the dotted line part of Fig. 1(a). Therefore, we can selectively apply the method to the partial circuitry of the existing synchronous circuit.

(3) The proposed method must generate the multiple clock pulse and the enable signal during one clock period. Therefore, it may be difficult to apply it a very high speed circuit. The limitation of the proposed method is one of future works. However, the proposed method is applicable

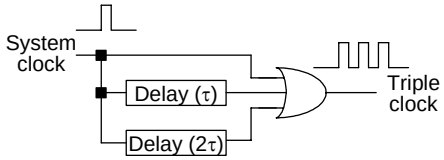

Fig. 7(a) Triple clock generator (1).

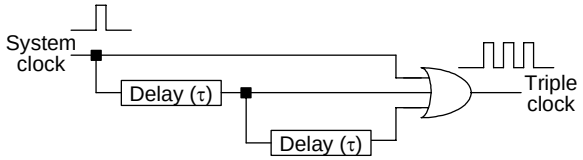

Fig. 7(b) Triple clock generator (2).

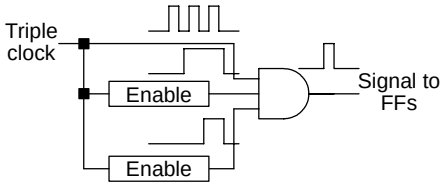

Fig. 8(a) Triple-to-single clock detector (1).

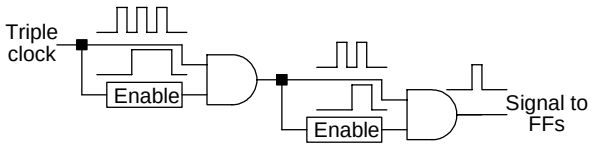

Fig. 8(b) Triple-to-single clock detector (2).

to not only LSIs but also every synchronous circuit including board circuits. Besides, it is useful for circuits demanded high reliability. Therefore, we believe that the proposed method is still valuable.

4. Conclusions

We have proposed a method for generating/detecting clock signals with tolerance for crosstalk noises. We solved the problem of the crosstalk pulse generated on the clock signal by using the multiple clock pulse. We showed one example implemented our idea and its effectiveness by circuit simulation. The circuit realized our idea is easy built in the conventional synchronous circuit as an adapter circuit. Although we considered the crosstalk faults, the proposed method is also applicable to transient faults generated on the clock line.

In order to show practicality, we further examine circuit performance including area overhead and variations of manufacturing and power supplies, other simple and useful implementation, and design limitation of the proposed method.

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